UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,877	09/28/2001	Patrick L. Ferguson	COMP:0247 P01-3710	3577

7590 03/09/2005

Michael G. Fletcher
Fletcher, Yoder & Van Someren
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER	
DUNCAN, MARC M	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,877	FERGUSON ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-19* is/are allowed.

6)☒ Claim(s) *1-4,6-9,11,30 and 31* is/are rejected.

7)☒ Claim(s) *5,10 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

Status of the Claims

Claims 11, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig et al.

Claims 1-4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. in view of Abe et al.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig and Abe as applied to claim 1 above and further in view of Krueger.

Claims 5, 10 and 32-34 are objected to.

Claims 12-19 are allowed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig et al.

Regarding claim 11:

Olarig teaches the memory system comprising a plurality of memory cartridges, comprising the act of independently transitioning each of the plurality of memory cartridges to a redundant-ready state in Fig. 2, col. 1 lines 39-46 and col. 9 lines 55-63. When the memory module is powered and the connector is live, the memory module is

used in a redundant, fault tolerant scheme. It is clear, therefore, that the state of being connected, i.e. the first state, is a redundant-ready state as claimed.

Regarding claim 30:

Olarig teaches wherein act of independently transitioning each of the plurality of memory cartridges to a redundant-ready state comprises the act of independently transitioning each of the plurality of memory cartridges to a redundant-ready state from a powerdown state in col. 1 lines 39-46 and col. 9 lines 55-63. When a slot connector is connected after the removal and insertion of a memory cartridge, the memory cartridge is integrated into the fault tolerant scheme, i.e. transitioned to a redundant ready state from a powerdown state.

Regarding claim 31:

Olarig teaches wherein act of independently transitioning each of the plurality of memory cartridges to a redundant-ready state comprises the act of independently transitioning each of the plurality of memory cartridges to a redundant-ready state from a powerup state in col. 1 lines 39-46 and col. 9 lines 55-63. The powerup state is clearly an intermediate state between powerdown and redundant-ready.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. in view of Abe et al.

Regarding claim 1:

Olarig teaches a memory system comprising a plurality of memory cartridges in Fig. 2.

Olarig teaches a data controller comprising a plurality of control mechanisms, each of the control mechanisms configured to independently interpret the transition of the corresponding memory cartridge between a first state of operation and a second state of operation, wherein the first state of operation permits the memory cartridge to be used to store data in a redundant memory array and wherein the second state of operation prevents the memory cartridge from being used to store data in a redundant memory array in Fig. 2, Fig. 5, col. 1 lines 39-46 and col. 9 lines 55-63. When the memory module is powered and the connector is live, the memory module is used in a redundant, fault tolerant scheme. It is clear, therefore, that the state of being connected, i.e. the first state, is a redundant-ready state as claimed. The second state, when not connected, does not allow the memory to be used to store data in a redundant

memory array. The data controller is responsible for transitioning each of the memory modules and therefore contains a control mechanism associated with each of the memory modules.

Olarig does not explicitly teach each of the plurality of memory cartridges comprising at least one memory device and a memory controller. Olarig does not explicitly teach the control mechanisms corresponding to a respective one of the memory controllers because Olarig does not explicitly teach each of the plurality of memory cartridges comprising at least one memory device and a memory controller. Olarig does, however, teach a plurality of memory cartridges.

Abe teaches each of the plurality of memory cartridges comprising at least one memory device and a memory controller in paragraph 0076-paragraph 0078.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the memory cartridges of Abe with the hot plug memory system of Olarig.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the memory cartridges of Abe allow the memories to be hot swapped and allow for protection of crucial data contained in the memory cartridges, both explicitly stated needs of Olarig.

Regarding claim 2:

Olarig teaches wherein the at least one memory device comprises a dual inline memory module (DIMM) in col. 8 line 66.

Regarding claim 3:

Olarig teaches wherein the first state of operation comprises a redundant-ready state of operation in col. 1 lines 39-46 and col. 9 lines 55-63. When the memory module is powered and the connector is live, the memory module is used in a redundant, fault tolerant scheme. It is clear, therefore, that the state of being connected, i.e. the first state, is a redundant-ready state as claimed.

Regarding claim 4:

Olarig teaches wherein the memory system is configured to operate in a redundant mode when each of the plurality of memory cartridges is in the redundant-ready state in col. 9 lines 55-63.

Regarding claim 6:

Olarig teaches wherein the plurality of memory cartridges comprises five memory cartridges in Fig. 2. Olarig pictures a plurality of memory cartridges. Five memory cartridges are, therefore, implicitly taught.

Regarding claim 8:

Abe teaches wherein each memory controller is configured to control access to the at least one memory device on the corresponding memory cartridge in paragraph 0078.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig and Abe as applied to claim 1 above and further in view of Krueger.

Regarding claim 7:

The teachings of Olarig and Abe are outlined above.

Olarig and Abe do not explicitly teach wherein at least one of the plurality of memory cartridges is configured to store parity data. Olarig and Abe do, however, teach a fault tolerant array of memory cartridges.

Krueger teaches wherein at least one of the plurality of memory cartridges is configured to store parity data in Fig. 1 and the Abstract lines 1-5.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the parity teachings of Krueger with the fault tolerant array of Olarig and Abe.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Olarig and Abe explicitly state the need for a fault tolerant array in which data can be reconstructed for a replacement memory module. The parity data storage of Krueger meets this explicitly stated need.

Regarding claim 9:

The teachings of Olarig and Abe are outlined above.

Olarig and Abe do not explicitly teach wherein the data controller writes data in a striped fashion across the plurality of memory cartridges. Olarig and Abe do, however, teach a fault tolerant array of memory cartridges.

Krueger teaches wherein the data controller writes data in a striped fashion across the plurality of memory cartridges in the Abstract lines 21-24.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the striping teachings of Krueger with the fault tolerant array of Olarig and Abe.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Olarig and Abe explicitly state the need for a fault tolerant array in which data can be reconstructed for a replacement memory module. The striping of data taught by Krueger meets this explicitly stated need.

Allowable Subject Matter

Claims 5, 10 and 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 11/30/2004 have been fully considered but they are not persuasive.

Regarding applicant's argument that Olarig does not contain memory cartridges, the examiner respectfully disagrees. A cartridge, as defined in the Third Edition of the Microsoft Press Computer Dictionary, is "any of various container devices that usually consist of some form of plastic housing." The memory modules of Olarig are clearly containers that house a plurality of chips on a plastic board. The memory cartridges of the instant claims, given their broadest reasonable interpretation as found in the Microsoft Dictionary, clearly read on the Olarig reference.

Regarding applicant's argument that the Olarig reference does not teach the independently transitioning the plurality of memory cartridges, the examiner disagrees. It has been established above that the memory cartridges read on the Olarig reference.

The Olarig reference teaches transitioning each of the memory modules independently. The language of the instant claim therefore clearly reads on the Olarig reference.

Regarding applicant's argument that the Olarig reference does not teach a plurality of control mechanisms, the examiner disagrees. The Olarig reference clearly teaches interpreting the transitioning of each of the memory modules independently. This interpreting is clearly done by a control mechanism. The transitioning is interpreted independently for a plurality of memory devices and therefore clearly requires multiple control mechanisms. When the Olarig reference is combined with the Abe reference, each of the memory devices contains a memory controller and it is therefore clearly seen that the combination would result in each of the control mechanisms being associated with a respective memory controller.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

Bryce P. Bonzo
Bryce P. Bonzo
Primary Examiner
AU 2114